Claim(s)

Sub A3

1. An interposer for connecting a chip die directly to a circuit card comprising a layer of elastic dielectric material having an array of metal plated vias extending from one surface to the other each terminating in a metal pad with said vias sloped with respect to said surfaces.

2. The interposer as set forth in Claim 1 wherein said array of metal plated vias each terminating in a metal pad is an array of copper plated vias each terminating in a copper pad.

3. The interposer as set forth in Claim 2 wherein said elastic dielectric material has an array of holes therethrough positioned between said array of copper plated vias.

4. The interposer as set forth in Claim 3 wherein said elastic dielectric material is 10 to 15 mils thick and has an elastic modulus in the range of 50,000 to 400,000 psi.

Sub A4

5. An electronic package comprising:

a semiconductor chip die having an array of conductive pads on one surface thereof;

a flexible layer of dielectric material having an array of metal plated vias extending therethrough to opposing surfaces thereof with said array

corresponding to said array of conductive pads on said chip die and with each of said vias terminating in a metal pad on each of said opposing surfaces with each said metal pad on one of said surfaces connected by solder to respective ones of said array of conductive pads on said chip die; and

a circuit card having an array of conductive pads corresponding to said array of metal pads on the other of said surfaces of said flexible layer and connected by solder thereto.

6. The electronic package of Claim 5 wherein said array of metal plated vias each terminating in a metal pad is an array of copper plated vias each terminating in a copper pad.

7. The electronic package of Claim 5 wherein said copper plated vias of said flexible layer are formed by two segments each sloped with respect to an opposing surface and meeting internal to said surfaces to form a V-shaped copper plated via.

8. The electronic package of Claim 5 wherein the said copper plated vias of said flexible layer are sloped with respect to said opposing surfaces of said layer.

9. The electronic package of Claim 5 wherein said flexible layer has an array of holes therethrough positioned between said array of copper plated vias.

10. The electronic package of Claim 5 wherein said copper pads on said one of said surfaces is connected to said array of conductive pads on said chip die by a copper plated connection.

11. The electronic package of Claim 5 wherein said flexible layer is a low elastic modulus material.

12. The electronic package of Claim 5 wherein said flexible layer has an elastic modulus in the range of 50,000 to 400,000 psi.

13. The electronic package of Claim 5 wherein said copper plated vias are filled with solder.

14. A method of connecting a semiconductor chip die having an array of conductive pads on one surface thereof to a circuit card having a corresponding array of conductive pads, comprising the steps of:

forming a flexible interposer to electrically connect said chip die to a circuit card by forming an array of metal plated vias in a layer of flexible material positioned to correspond to said array of conductive pads on said chip die with each via terminating on opposing surfaces of said layer of flexible material in metal connection pads;

attaching first solder bumps to each pad of said array of conductive pads on said one surface of said chip die;

positioning said flexible interposer so as to align and contact said array of metal pads on one surface of said flexible material with said first solder bumps attached to said conductive pads on said chip die;

heating said first solder bumps to melt and draw said solder into each of said metal plated vias to fill said vias to said metal pads on the other surface of said flexible material and electrically attach said array of metal pads on said one surface to said array of conductive pads on said chip die;

attaching second solder bumps to each pad of said metal pads on said other surface of said flexible material;

positioning the said array of conductive pads on said circuit card so as to align and contact said second solder bumps attached to said metal pads on said other surface of said flexible material; and

applying heat to said second solder bumps attached to the said metal pads on said other surface of said flexible material so as to melt said second solder bumps to electrically attach said array of metal pads on said other surface to said array of conductive pads on said circuit card.

15. The method as set forth in Claim 14 wherein said first solder bumps comprise a high melt solder.

16. The method as set forth in Claim 15 wherein said second solder bumps comprise a lower melt solder than said high melt solder.

17. The method as set forth in Claim 16 wherein said array of metal plated vias each terminating in a metal pad is an array of copper plated vias each terminating in a copper pad.

18. The method as set forth in Claim 17 wherein said layer of flexible material has an elastic modulus between about 50,000 to 400,000 psi.

19. The method as set forth in Claim 18 wherein said vias are sloped with respect to the surfaces of said layer of flexible material.

20. The method as set forth in Claim 14 wherein the step of forming a flexible interposer includes the additional step of forming an array of holes positioned between said array of copper plated vias.

21. A method of connecting a semiconductor chip die having an array of conductive pads on one surface thereof to a circuit card having a corresponding array of conductive pads, comprising the steps of:

laminating one surface of a layer of flexible dielectric material to said chip die;

forming an array of holes through said layer of flexible material at locations to expose said conductive pads on said chip die;

depositing metal in said array of holes to provide a conductive connection from said conductive pads on said chip die to conductive pads formed thereby on the other surface of said flexible material;

attaching solder bumps to said conductive pads on said other surface of said flexible material;

positioning said array of conductive pads on said circuit card so as to align and contact said solder bumps attached to said conductive pads on said other surface of said flexible material; and

applying heat to said solder bumps to electrically attach said array of conductive pads on said circuit card to said conductive pads on said other surface of said flexible material.

22. The method as set forth in Claim 21 wherein said lamination step comprises laminating in a lamination press at between 180 and 400°C and 250 and 2000 psi for at least 1 hour.